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TANG, KENNETH	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/728,649	**Applicant(s)** WANG ET AL.	
	Examiner KENNETH TANG	**Art Unit** 2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2008*.

2a)□ This action is **FINAL**. 2b)☒ This action is non-final.

3)□ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)□ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)□ Claim(s) _____ is/are objected to.

8)□ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)□ The specification is objected to by the Examiner.

10)□ The drawing(s) filed on _____ is/are: a)□ accepted or b)□ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)□ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)□ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)□ All b)□ Some * c)□ None of:

1.□ Certified copies of the priority documents have been received.

2.□ Certified copies of the priority documents have been received in Application No. _____.

3.□ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) □ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) □ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) □ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) □ Notice of Informal Patent Application

6) □ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination.

2. This action is in response to the Amendment/Remarks on 3/7/08. Applicant's arguments have been fully considered but are moot in view of the new grounds of rejections.

Claim Objections

3. Claim 14 is objected to because of the following informalities: "a switch handler to invoke a helper thread responsive to occurrence" should be changed to – a switch handler to invoke a helper thread responsive to the occurrence – in order to correct the grammar problem.

4. Claim 28 is objected to because of the following informalities: On line 9, "in response the user-defined trigger event" should be changed to – in response to the user-defined trigger event – in order to correct the grammar problem. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 18-27 and 29-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. As to claims 18, 20, 21, and 25, the term "minimal context information" is a relative term which renders the claim indefinite. The term "minimal context information" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Dependent claims 19, 22-24, and 26-27 are also rejected as being dependent upon rejected claims 18 and 21.

b. Claims 29-30 recite the limitation "The system" in line 1. There is insufficient antecedent basis for this limitation in the claim.

c. Claim 30 recites the limitation "the user-marking instruction" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 4-7, 10-12, 14-16, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (hereinafter Wang) (US 2002/0144083 A1).

7. As to claim 1, Wang teaches an apparatus comprising:

a trigger-response mechanism that includes at least one bank of user-programmable registers to identify a user-defined trigger event (page 3, [0044]); and

a thread switch handler coupled to the trigger-response mechanism, the thread switch handler to invoke a second instruction stream responsive to an indication from the trigger-response mechanism that the user-defined trigger event has occurred during execution of a first instruction stream (switching from main thread to the spawned speculative thread via triggers) (Abstract, page 4, [0055], page 5, [0065]).

8. As to claim 4, Wang teaches wherein the thread switch handler is to save an instruction pointer address for the first instruction stream before invoking the second instruction stream (page 4, [0064]).

9. As to claim 5, Wang further comprising: a task queue to receive the instruction pointer address (Fig. 1, item 110, [0080], [0085]).

10. As to claim 6, Wang teaches wherein: the task queue further comprises a memory location (page 3, [0044]).

11. As to claim 7, Wang teaches wherein: the task queue further comprises a register (page 3, [0044]).

12. As to claim 10, Wang teaches wherein the thread switch handler is to save context information for the first instruction stream before invoking the second instruction stream (page 4, [0064]).

13. As to claim 11, Wang teaches wherein: the thread switch handler is further to save context for the first instruction stream in a memory location before invoking the second instruction stream (page 3, [0044]).

14. As to claim 12, Wang teaches wherein: the thread switch handler is further to save context for the first instruction stream in a register before invoking the second instruction stream (page 3, [0044]).

15. As to claim 14, Wang teaches a system comprising:

a memory to hold an instruction (registers) (page 3, [0044], lines 1-10); and

a processor coupled to the memory (registers are coupled to the processor) (Fig. 1, items 100, 102, 112), including raw event detection logic to detect at least one raw event, a user-addressable register to specify a user-defined trigger event based on the at least one raw event, a switch handler to invoke a helper thread (spawning a speculative thread via an event trigger) responsive to the occurrence of the user-defined trigger event (Abstract, page 3, [0047], page 5, [0065]).

16. As to claim 15, Wang teaches wherein: the instruction includes a marking instruction, when executed, to specify the user-defined trigger event in the user-addressable register (page 4, [0055], lines 1-8).

17. As to claim 16, Wang teaches wherein: the instruction is a trigger instruction; and raw event detection logic is to detect an opcode of the trigger instruction when the trigger instruction reaches an execution phase of an execution pipeline (page 2, [0032] and [0037]).

18. As to claim 18, Wang teaches wherein: the switch handler is further to maintain minimal context information for a current thread before invoking the helper thread, wherein the minimal context information excludes traditional context information (page 4, [0061]).

19. As to claim 19, Wang teaches wherein: the excluded traditional context information further comprises general register values (page 3, [0044]).

20. As to claim 20, Wang teaches wherein the minimal thread context information comprises an instruction pointer address value (page 6, [0085], lines 5-9).

21. Claims 21-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Kissell (US 2005/0050395 A1).

22. As to claim 21, Kissell teaches a method comprising:

detecting a trigger condition (a miss occurrence or if thread 212 stalls, for example) (page 1, [0011], lines 14-23);

suspending execution of a first thread on a single-threaded processor (thread to be suspended and another thread activated) (page 2, [0014], lines 3-4);

utilizing hardware to save minimal context information (minimum possible overhead) for the current thread without operating system intervention (page 2, [0020], lines 4-8); and

invoking a second thread on the single-threaded processor without operating system intervention (creating thread by using a FORK command or switching from one thread to another) (page 2, [0020], lines 6-10, page 1, [0013], lines 2-4).

23. As to claim 23, Kissell teaches wherein: detecting a user-specified trigger condition further comprises determining that an asynchronous condition specified in a marking instruction (privileged instruction, etc.) has been encountered (page 6, [0093] and [0097]).

24. As to claim 24, Kissell teaches wherein the minimal thread context information comprises an instruction pointer address value (page 8, [0133]).

25. As to claim 25, Kissell teach further comprising: determining that the first thread should be resumed; restoring the minimal context information for the first thread; and resuming execution of the first thread without operating system intervention (page 5, [0085], page 6, [0104], lines 1-13).

26. As to claim 27, Kissell teaches wherein detecting a user-specified trigger condition further comprises: generating an asynchronous response to indicate that the second thread should be invoked (page 6, [0093]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

> such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claims 1-4 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. (hereinafter Ahmad) (US 7,010,672 B2) in view of Ranganathan (US 6,098,169).

28. As to claim 1, Ahmad teaches an apparatus comprising:

a trigger-response mechanism (breakpoint/watchpoint circuit and programmable trigger logic circuit) that includes at least one bank of user-programmable registers to identify a user-defined trigger event (plurality of trigger event detection registers that generate pre-trigger signals in response to user-defined trigger events) (col. 2, lines 36-67, Abstract).

29. Ahmad is silent in teaching a thread switch handler coupled to the trigger-response mechanism, the thread switch handler to invoke a second instruction stream responsive to an indication from the trigger-response mechanism that the trigger event has occurred during execution of a first instruction stream. However, Ranganathan discloses an event trigger-response mechanism using a thread switch handler to detect when the switching between a first and second thread occurs based on the contexts of the registers, wherein the first and second threads each include a series of instructions (see Abstract, col. 2, lines 25-38, col. 3, lines 11-21). Ahmad and Ranganathan are analogous art because they are both in the same field of endeavor of event detection in a computer processing system. One of ordinary skill in the art would have known to modify Ahmad's trigger-response mechanism that is based on events such that it would include the thread switch handler from Ranganathan. The suggestion/motivation for doing so

would have been to provide the predicted result of being able to track and monitor processor events, at the software thread level and so that negative/adverse processes or threads of the event can be identified and corrected (col. 1, lines 11-12, col. 2, lines 64-67 through col. 3, lines 1-8). Therefore, it would have been obvious to one of ordinary skill in the art to combine Ahmad and Ranganathan to obtain the invention of claim 1.

30. As to claims 2-3, Ahmad and Ranganathan teach wherein the thread switch handler is further to invoke the second instruction stream responsive to an indication from the trigger-response mechanism that a user-defined trigger event has occurred during execution of the first instruction stream (see rejection of claim 1). However, Ahmad and Ranganathan are silent in synchronous and asynchronous triggering of events. However, Official Notice is taken that synchronous and asynchronous processing are well known and with each having distinct advantages. For example, asynchronous processing returns control to the user program without waiting for an I/O to complete. The I/O then can continue while other system operations occur. On the other hand, synchronous processing returns the control to the user process and is more simpler than asynchronous processing. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ahmad and Ranganathan to include the features of synchronous and asynchronous processing to achieve the benefit as described above.

31. As to claim 4, Ahmad teaches wherein the thread switch handler is to save an instruction pointer address for the first instruction stream before invoking the second instruction stream (Fig. 2, item 121, 147).

32. As to claim 10, Ranganathan teaches wherein the thread switch handler is to save context information for the first instruction stream before invoking the second instruction stream (col. 3, lines 11-19). In context switching between the first thread and the second thread, the state/context is stored and then later restored.

33. As to claim 11, Ranganathan teaches wherein: the thread switch handler is further to save context for the first instruction stream in a memory location before invoking the second instruction stream (col. 3, lines 11-19). In context switching between the first thread and the second thread, the state/context is stored in a memory location and then later restored.

34. As to claim 12, Ranganathan teaches wherein: the thread switch handler is further to save context for the first instruction stream in a register before invoking the second instruction stream (col. 3, lines 11-19). In context switching between the first thread and the second thread, the state/context is stored in a memory location and then later restored.

35. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (hereinafter Wang) (US 2002/0144083 A1).

36. As to claims 2-3, Wang teach wherein the thread switch handler is further to invoke the second instruction stream responsive to an indication from the trigger-response mechanism that a user-defined trigger event has occurred during execution of the first instruction stream (see rejection of claim 1). However, Wang is silent in synchronous and asynchronous triggering of events. However, Official Notice is taken that synchronous and asynchronous processing are well known and with each having distinct advantages. For example, asynchronous processing returns control to the user program without waiting for an I/O to complete. The I/O then can continue while other system operations occur. On the other hand, synchronous processing returns the control to the user process and is more simpler than asynchronous processing. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ahmad and Ranganathan to include the features of synchronous and asynchronous processing to achieve the benefit as described above.

37. Claims 14, 16, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. (hereinafter Ahmad) (US 7,010,672 B2) in view of Marcuello et al. (hereinafter Marcuello) ("Thread-Spawning Schemes for Speculative Multithreading", IEEE, 2000).

38. As to claim 14, Ahmad teaches a system comprising:

a memory to hold an instruction (Fig. 2, items 147, 149); and

a processor coupled (Processor 300) to the memory (registers are coupled to the processor), including raw event detection logic to detect at least one raw event, a user-addressable register to specify a user-defined trigger event based on the at least one raw event (col. 2, lines 36-67, Abstract).

39. Ahmad is silent in having a switch handler that invokes a helper thread responsive to the occurrence of trigger event. However, Marcuello discloses spawning a thread (creating a helper thread) from the event occurrence of when a spawning point is reached (see page 1, under 1. Introduction, paragraphs 4-5), pages-2, Section 3. Speculative Thread-Level Parallelism). One of ordinary skill in the art would have known to modify Ahmad's event detection logic such that it would spawn a helper thread in the event of when a spawning point is reached. The suggestion/motivation for doing so would have been to provide the predicted result of improved processor performance from parallelism (see Abstract and 1. Introduction). Therefore, it would have been obvious to one of ordinary skill in the art to combine Ahmad and Marcuello to obtain the invention of claim 14.

40. As to claim 16, Ahmad teaches wherein: the instruction is a trigger instruction; and the trigger-response mechanism is further to detect the opcode of the trigger instruction when the

trigger instruction reaches an execution phase of an execution pipeline (col. 2, lines 1-16, col. 9, lines 1-32).

41. As to claim 18, Ahmad teaches wherein: the switch handler is further to maintain minimal context information for a current thread before invoking the helper thread, wherein the minimal context information excludes traditional context information (Fig. 2, items 147, 149).

42. As to claim 19, Ahmad teaches the excluded traditional context information comprises general register values (Fig. 2, items 147, 149).

43. As to claim 20, Ahmad teaches wherein the minimal thread context information comprises an instruction pointer address value (Fig. 2, item 121).

44. **Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. (hereinafter Ahmad) (US 7,010,672 B2) in view of Ranganathan (US 6,098,169), and further in view of Nojiri (US 5,179,685).**

45. As to claim 5, Ahmad and Ranganathan are silent in further comprising: a task queue to receive the instruction pointer address. However, Nojiri teaches using a task queue so that task

control blocks for respective blocks are linked together by register bank pointers (col. 4, lines 35-43). Nojiri teaches that this results in task/context switching that can be realized without erroneous operation (col. 4, lines 43-45). One of ordinary skill in the art would have known to modify Ahmad and Ranganathan to include the feature of a task queue to receive the instruction pointer address. The suggestion/motivation for doing so would have been to allow for context switching to be realized and for the registers to be obtained without erroneous operation, as stated in Nojiri (col. 4, lines 43-45, col. 5, lines 1-22). Therefore, it would have been obvious to combine Nojiri with the references of Ahmad and Ranganathan to obtain the invention of claim 5.

46. As to claim 6, Nojiri teaches wherein: the task queue further comprises a memory location (col. 4, lines 43-45, col. 5, lines 1-22).

47. As to claim 7, Nojiri teaches wherein: the task queue further comprises a register (register bank or register sets) (col. 5, lines 1-22).

48. **Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. (hereinafter Ahmad) (US 7,010,672 B2) in view of Ranganathan (US 6,098,169), and further in view of Hugly (US 2002/0138706 A1).**

49. As to claim 8, Ahmad and Ranganathan are silent in further comprising: a plurality of event counters coupled to the trigger-response mechanism, wherein each event counter is to detect an atomic processor event. However, Hugly teaches exception handling and context switching wherein a plurality of event counters are coupled to the switching mechanism, wherein each event counter detects an atomic processor event ([0041]-[0043], [0045]). One of ordinary skill in the art would have known to modify Ahmad and Ranganathan to include using a plurality of event counters. The motivation/suggestion for doing so would have been to improve the handling of any access conflicts, thus improving control and reducing overheard, as stated in Hugly ([0008]). Therefore, it would have been obvious to combine Hugly with Ahmad and Ranganathan to obtain the invention of claim 8.

50. **Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (hereinafter Wang) (US 2002/0144083 A1) in view of Hugly (US 2002/0138706 A1).**

51. As to claim 8, Wang is silent in further comprising: a plurality of event counters coupled to the trigger-response mechanism, wherein each event counter is to detect an atomic processor event. However, Hugly teaches exception handling and context switching wherein a plurality of event counters are coupled to the switching mechanism, wherein each event counter detects an atomic processor event ([0041]-[0043], [0045]). One of ordinary skill in the art would have known to modify Ahmad and Ranganathan to include using a plurality of event counters. The

motivation/suggestion for doing so would have been to improve the handling of any access conflicts, thus improving control and reducing overheard, as stated in Hugly ([0008]). Therefore, it would have been obvious to combine Hugly with Wang to obtain the invention of claim 8.

52. As to claim 9, Wang teach wherein the thread switch handler is further to invoke the second instruction stream responsive to an indication from the trigger-response mechanism that an asynchronous user-defined trigger event has occurred during execution of the first instruction stream (see rejection of claim 1). Hugly teaches trigger events being based on one or more of the atomic processor events ([0041]-[0043], [0045]).

53. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. (hereinafter Ahmad) (US 7,010,672 B2) in view of Ranganathan (US 6,098,169), and further in view of Spix et al. (hereinafter Spix) (US 6,195,676).

54. As to claim 13, Ahmad and Ranganathan teach further comprising: one or more user-programmable control registers coupled to the thread switch handler (see rejection of claim 1). Ahmad and Ranganathan are silent in teaching the value of the one or more control registers to indicate the weight of context information. However, Spix teaches context switching wherein the amount of context information in the registers are indicated and classified as lightweight, for

example (col. 3,lines 9-35, col. 14, lines 66-67 through col. 15, lines 1-6). One of ordinary skill in the art would have known to modify Ahmad and Ranganathan to include Spix's feature of identifying weights of context information for the use of context switching. The motivation/suggestion for doing so would have been to minimize total context switch overhead and minimizing the delays and bottlenecks by classifying the amount of context information (weights) and context switching according to those weights (col. 3,lines 9-35, col. 14, lines 66-67 through col. 15, lines 1-6). Therefore, it would have been obvious to combine Spix with Ahmad and Ranganathan to obtain the invention of claim 13.

55. Claims 13, 17, and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (hereinafter Wang) (US 2002/0144083 A1) in view of Spix et al. (hereinafter Spix) (US 6,195,676).

56. As to claim 13, Wang teach further comprising: one or more user-programmable control registers coupled to the thread switch handler (see rejection of claim 1). Wang is silent in teaching the value of the one or more control registers to indicate the weight of context information. However, Spix teaches context switching wherein the amount of context information in the registers are indicated and classified as lightweight, for example (col. 3,lines 9-35, col. 14, lines 66-67 through col. 15, lines 1-6). One of ordinary skill in the art would have known to modify Ahmad and Ranganathan to include Spix's feature of identifying weights of context information for the use of context switching. The motivation/suggestion for doing so

would have been to minimize total context switch overhead and minimizing the delays and bottlenecks by classifying the amount of context information (weights) and context switching according to those weights (col. 3,lines 9-35, col. 14, lines 66-67 through col. 15, lines 1-6). Therefore, it would have been obvious to combine Spix with Wang to obtain the invention of claim 13.

57. As to claim 17, it is rejected for the same reasons as stated in the rejection of claim 13.

58. As to claim 28, Wang teaches a processor comprising:

event detection logic to detect a raw event (switch-on-event based on event triggers) (page 2, [0030], [0047]);

user-programmable event logic coupled to the event detection logic to indicate a user-defined trigger event, the user-defined trigger event to be based on at least the raw event (page 5, [0065]);

thread switch logic coupled to the user-programmable event logic and context control logic, the thread switch logic, in response the user-defined trigger event being detected, to save a portion of a first context to be saved that is to be specified in the user-programmable context control logic and to spawn a helper thread without operating system intervention (page 5, [0064]-[0065]).

59. Want is silent in taking into consideration the weight of the context. However, Spix teaches context switching wherein the amount of context information in the registers are indicated and classified as lightweight, for example (col. 3,lines 9-35, col. 14, lines 66-67 through col. 15, lines 1-6). One of ordinary skill in the art would have known to modify Ahmad and Ranganathan to include Spix's feature of identifying weights of context information for the use of context switching. The motivation/suggestion for doing so would have been to minimize total context switch overhead and minimizing the delays and bottlenecks by classifying the amount of context information (weights) and context switching according to those weights (col. 3,lines 9-35, col. 14, lines 66-67 through col. 15, lines 1-6). Therefore, it would have been obvious to combine Spix with Wang to obtain the invention of claim 13.

60. As to claim 29, Wang teaches wherein the user-programmable event logic includes at least a user-programmable event register, and wherein the user-defined trigger event is to be programmed in the user-programmable event register in response to execution of a user marking instruction (page 4, [0055]). In addition, Spix teaches the use of marking instructions in event processing (col. 45, lines 37-53).

61. As to claim 30, Wang teaches further comprising trigger response logic coupled to the user-programmable event logic and the event detection logic to detect the user-defined trigger event based on at least the raw event, wherein the trigger response logic is to monitor for the

user-defined trigger event for a predetermined timeout period after execution of the user-marking instruction (page 3, [0047], lines 6-20).

62. Claims 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. (hereinafter Ahmad) (US 7,010,672 B2) in view of Marcuello et al. (hereinafter Marcuello) ("Thread-Spawning Schemes for Speculative Multithreading", IEEE, 2000), and further in view of Spix (US 6,195,676).

63. As to claim 15, Marcuello and Ahmad teach the invention of claim 14. Marcuello and Ahmad are silent in teaching wherein: the instruction includes a marking instruction. Spix teaches the use of marking instructions in event processing (col. 45, lines 37-53). It would have been obvious to one of ordinary skill in the art to modify Marcuello and Ahmad to include marking instructions in order to separate/distinguish certain instructions to improve organization and efficiency of execution.

64. As to claim 17, Marcuello and Ahmad teach the invention of claim 14. In addition, Ahmad and Ranganathan are silent in teaching the value of the one or more control registers to indicate the weight of context information. However, Spix teaches context switching wherein the amount of context information in the registers are indicated and classified as lightweight, for example (col. 3,lines 9-35, col. 14, lines 66-67 through col. 15, lines 1-6). One of ordinary skill in the art would have known to modify Ahmad and Marcuello to include Spix's feature of

identifying weights of context information for the use of context switching. The motivation/suggestion for doing so would have been to minimize total context switch overhead and minimizing the delays and bottlenecks by classifying the amount of context information (weights) and context switching according to those weights (col. 3,lines 9-35, col. 14, lines 66-67 through col. 15, lines 1-6). Therefore, it would have been obvious to combine Spix with Ahmad and Marcuello to obtain the invention of claim 17.

Response to Arguments

65. Applicant's arguments have been fully considered but are moot in view of the new grounds of rejections.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- **Circenis (US 7,047,533 B2)** discloses the monitoring of a predetermined timeout period so that wait time would be reduced and be more flexible (see Abstract, col. 1, lines 10-37).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth Tang/
Examiner, Art Unit 2195

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195